REMARKS

Claim 9 has been amended and new claims 10-12 have been added. The application contains claims 9-12. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

The specification has been amended to insert the issued patent number for the corresponding parent application. No new matter has been introduced.

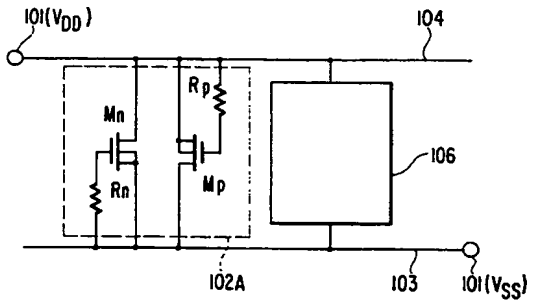
Claim 9 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Hirata, U.S. Patent no. 5,449,940. The rejection is respectfully traversed and reconsideration is respectfully requested.

Claim 9 recites a semiconductor apparatus formed on a semiconductor substrate. The apparatus comprises one or more outer ESD elements. Each ESD element comprises "a first terminal electrically connected between a first diffusion region and a higher voltage level of a main power supply; a second terminal electrically connected between a second diffusion region and a lower voltage level of the main power supply; and a third terminal electrically connected between a third diffusion region and said external connection terminals." The "first, second and third diffusion regions [are] formed separately from each other on said substrate." According to claim 9, "said third diffusion region causing electrostatic noise to be discharged through one of said first and second diffusion regions."

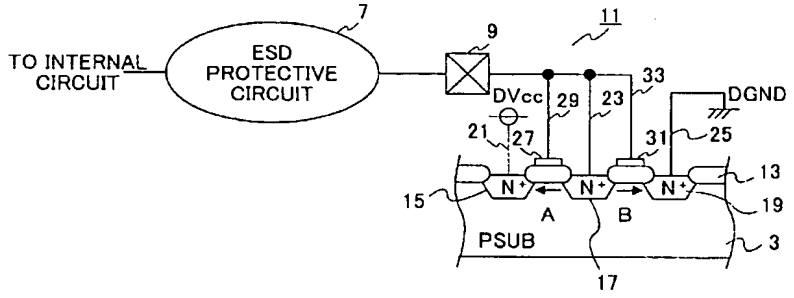
Applicant respectfully submits that Hirata fails to disclose the claimed invention. For example. Hirata discloses an integrated circuit having an N channel MOSFET Mn and a P channel MOSFET Mp connected in parallel to each other. The MOSFETs Mn, Mp are also connected between a power supply wiring 104 and a ground wiring 103. As shown below in Hirata's Figure 2, the gate electrode of the N

channel MOSFET Mn is connected to the ground wiring 103, while the gate electrode of the P channel MOSFET Mp is connected to the power supply wiring 104.

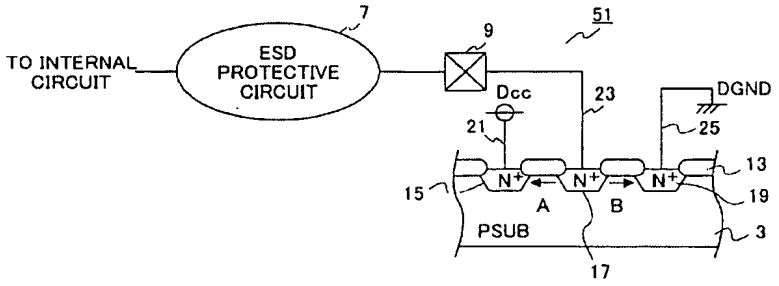
FIG. 2



Thus, the Hirata configuration is completely different than the claimed invention, which uses three separate terminals connected to three separate diffusion regions in a manner that allows the third diffusion region to cause "electrostatic noise to be discharged through one of said first and second diffusion regions." Hirata, unlike the claimed invention, needs two gate electrodes to operate two separate MOSFETs (totaling at least 6 diffusion regions) to provide ESD protection. An embodiment of the claimed invention is illustrated below.



In addition, as shown on the next page, the claimed invention can provide ESD protection even in the absence of gate electrodes, see e.g., Specification p. 17, lines 13-15 and Figure 7, Hirata cannot.



Accordingly, for at least the reasons set forth above, Applicant respectfully submits that claim 9 is allowable over Hirata. The rejection should be withdrawn and claim 9 allowed.

Claims 10-12 have been added and depend from claim 9 and are believed to be allowable along with claim 9 for at least the reasons set forth above and on their own merits.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

By _____

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